



SM3-4B4G6LSF8LH-FB
4GB DDR3L SODIMMs
512M x 8 Chips

DDR3L SYNCHRONOUS DRAM MODULE

DESCRIPTION

Using only pre-screened high performance ICs, this module has been tested and verified to be reliable running at DDR3 1600MHz low latency timing of 11-11-11 at 1.35V

FEATURES

- 204-pin, small-outline dual in-line memory module (SODIMM)
- DDR3 functionality and operations supported as defined in the component data sheet
- 4GB (512 Meg x 64)
- $V_{DD} = +1.35V$ (1.238-1.45V)
- $V_{DD} = +1.5V$ (1.425-1.575V)
- $V_{DDSPD} = +3.0V$ to +3.6V
- Fast data transfer rates: PC3-12800
- Nominal and dynamic on-die termination (ODT) for data, strobe, and mask signals
- Low-power auto self refresh (LPASR)
- Data bus inversion (DBI) for data bus
- On-die V_{REFDQ} generation and calibration
- On-board I²-C serial presence-detect (SPD) EEPROM
- Single-rank
- Fixed burst chop (BC) of 4 and burst length (BL) of 8 via the mode register set (MRS)
- Selectable BC4 or BL8 on-the-fly (OTF)
- Gold edge contacts
- Halogen-free
- Fly-by topology
- Terminated control command and address bus

SyncMAX Core Timing Parameters Table:

Speed Grade	Industry Nomenclature	Data Rate (MT/s)							t_{RCD}	t_{RP}	t_{RC}
		CL = 11	CL = 10	CL = 9	CL = 8	CL = 7	CL = 6	CL = 5	(ns)	(ns)	(ns)
FB	PC3-12800	1600	1333	1333	1066	1066	800	667	13.125	13.125	48.125

DIMENSIONS, ASSEMBLY DRAWING (TOP AND BOTTOM)

Figure 1 shows the placement of all the components on top and bottom layers of 512Megx64 4GB double sided module. 204-Pin DDR3 SODIMM

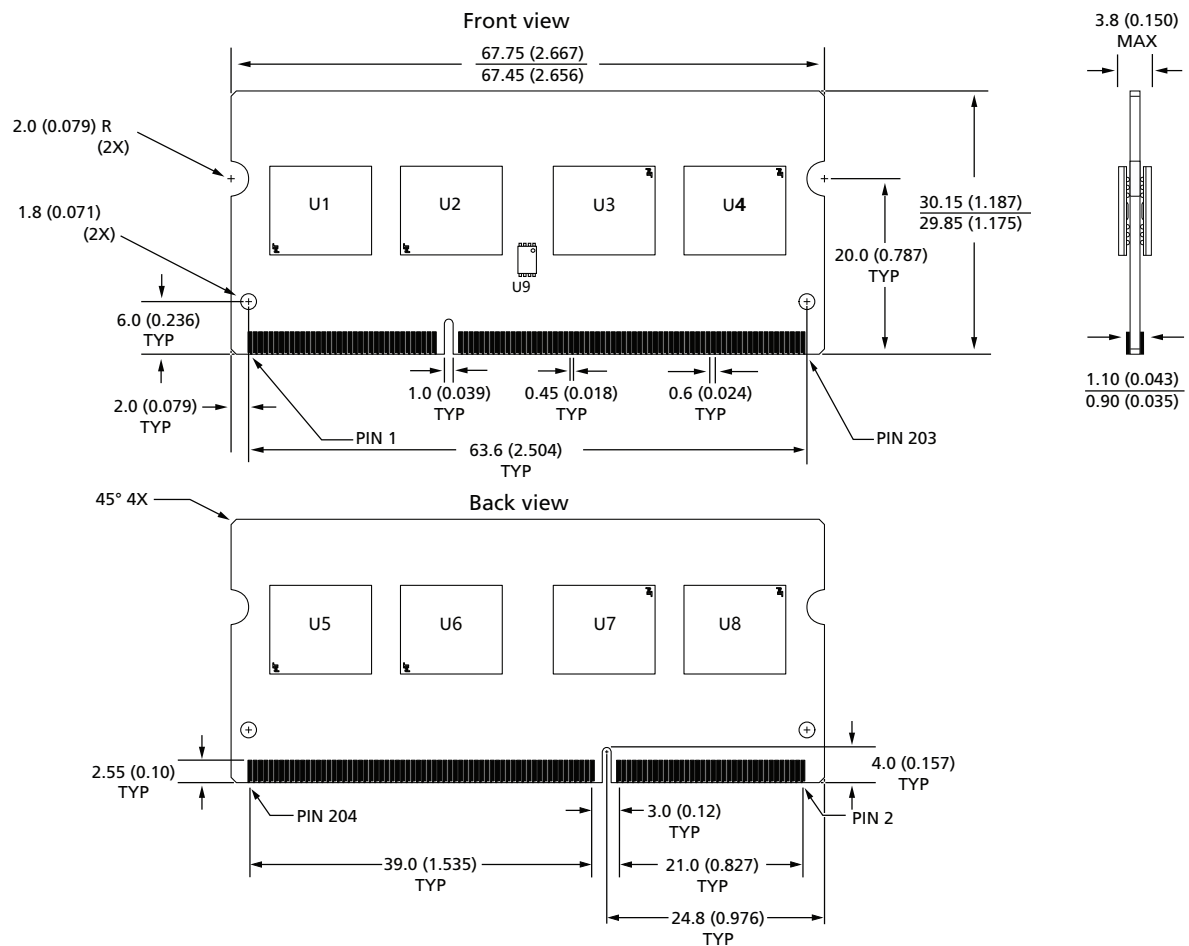
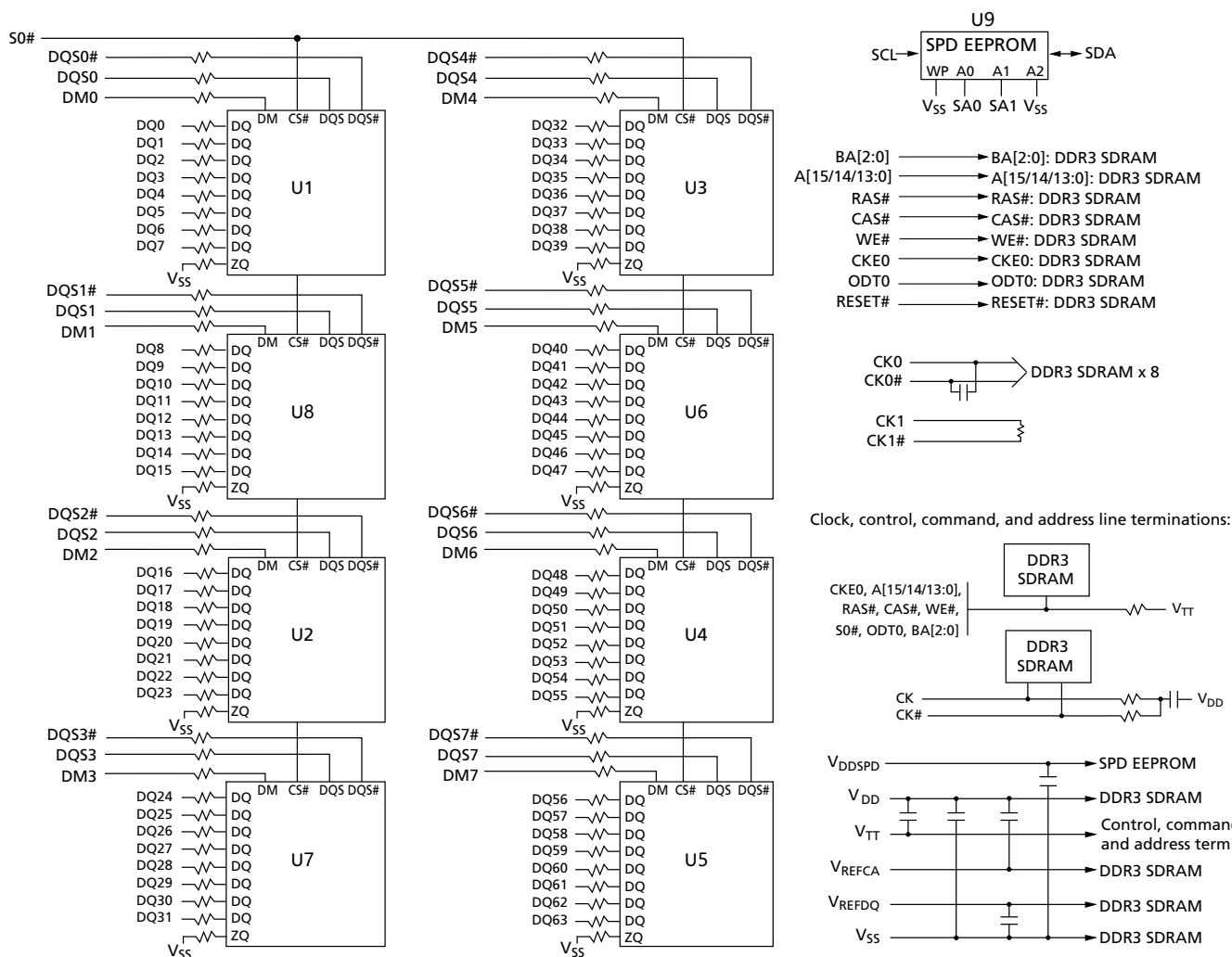


Figure 1

- Notes:
1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.
 2. The dimensional diagram is for reference only.

FUNCTIONAL BLOCK DIAGRAM

SyncMAX DDR3 (512Mx8 CHIPS)



Note: 1. The ZQ ball on each DDR3 component is connected to an external $240\Omega \pm 1\%$ resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.



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204-Pin DDR3 SODIMM Front								204-Pin DDR3 SODIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	V _{REFDQ}	53	DQ19	105	V _{DD}	157	DQ42	2	V _{SS}	54	V _{SS}	106	V _{DD}	158	DQ46
3	V _{SS}	55	V _{SS}	107	A10	159	DQ43	4	DQ4	56	DQ28	108	BA1	160	DQ47
5	DQ0	57	DQ24	109	BA0	161	V _{SS}	6	DQ5	58	DQ29	110	RAS#	162	V _{SS}
7	DQ1	59	DQ25	111	V _{DD}	163	DQ48	8	V _{SS}	60	V _{SS}	112	V _{DD}	164	DQ52
9	V _{SS}	61	V _{SS}	113	WE#	165	DQ49	10	DQ50#	62	DQ33#	114	S0#	166	DQ53
11	DM0	63	DM3	115	CAS#	167	V _{SS}	12	DQS0	64	DQS3	116	ODT0	168	V _{SS}
13	V _{SS}	65	V _{SS}	117	V _{DD}	169	DQS6#	14	V _{SS}	66	V _{SS}	118	V _{DD}	170	DM6
15	DQ2	67	DQ26	119	A13	171	DQS6	16	DQ6	68	DQ30	120	ODT1	172	V _{SS}
17	DQ3	69	DQ27	121	S1#	173	V _{SS}	18	DQ7	70	DQ31	122	NC	174	DQ54
19	V _{SS}	71	V _{SS}	123	V _{DD}	175	DQ50	20	V _{SS}	72	V _{SS}	124	V _{DD}	176	DQ55
21	DQ8	73	CKE0	125	NC	177	DQ51	22	DQ12	74	CKE1	126	V _{REFCA}	178	V _{SS}
23	DQ9	75	V _{DD}	127	V _{SS}	179	V _{SS}	24	DQ13	76	V _{DD}	128	V _{SS}	180	DQ60
25	V _{SS}	77	NC	129	DQ32	181	DQ56	26	V _{SS}	78	A15	130	DQ36	182	DQ61
27	DQS1#	79	BA2	131	DQ33	183	DQ57	28	DM1	80	A14	132	DQ37	184	V _{SS}
29	DQS1	81	V _{DD}	133	V _{SS}	185	V _{SS}	30	RESET#	82	V _{DD}	134	V _{SS}	186	DQS7#
31	V _{SS}	83	A12	135	DQS4#	187	DM7	32	V _{SS}	84	A11	136	DM4	188	DQS7
33	DQ10	85	A9	137	DQS4	189	V _{SS}	34	DQ14	86	A7	138	V _{SS}	190	V _{SS}
35	DQ11	87	V _{DD}	139	V _{SS}	191	DQ58	36	DQ15	88	V _{DD}	140	DQ38	192	DQ62
37	V _{SS}	89	A8	141	DQ34	193	DQ59	38	V _{SS}	90	A6	142	DQ39	194	DQ63
39	DQ16	91	A5	143	DQ35	195	V _{SS}	40	DQ20	92	A4	144	V _{SS}	196	V _{SS}
41	DQ17	93	V _{DD}	145	V _{SS}	197	SA0	42	DQ21	94	V _{DD}	146	DQ44	198	NF
43	V _{SS}	95	A3	147	DQ40	199	V _{DDSPD}	44	V _{SS}	96	A2	148	DQ45	200	SDA
45	DQS2#	97	A1	149	DQ41	201	SA1	46	DM2	98	A0	150	V _{SS}	202	SCL
47	DQS2	99	V _{DD}	151	V _{SS}	203	V _{TT}	48	V _{SS}	100	V _{DD}	152	DQS5#	204	V _{TT}
49	V _{SS}	101	CK0	153	DM5	-	-	50	DQ22	102	CK1	154	DQS5	-	-
51	DQ18	103	CK0#	155	V _{SS}	-	-	52	DQ23	104	CK1#	156	V _{SS}	-	-



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SPD EEPROM Operation

DDR3 SDRAM modules incorporate serial presence detect (SPD). The SPD data is stored in a 256-byte JEDEC standard JC-45-compliant EEPROM that remaining 128 bytes of storage are available for use by the customer. The SPD content is aligned with these blocks as shown in the table below.

Address Map (Cont'd)

Byte Number	Function Described	Notes
0	Number of Serial PD Bytes Written / SPD Device Size / CRC Coverage	1, 2
1	SPD Revision	
2	Key Byte / DRAM Device Type	
3	Key Byte / Module Type	
4	SDRAM Density and Banks	3
5	SDRAM Addressing	3
6	Module Nominal Voltage, VDD	
7	Module Organization	3
8	Module Memory Bus Width	
9	Fine Timebase (FTB) Dividend / Divisor	
10	Medium Timebase (MTB) Dividend	
11	Medium Timebase (MTB) Divisor	
12	SDRAM Minimum Cycle Time (tCKmin)	3
13	Reserved	
14	CAS Latencies Supported, Least Significant Byte	3
15	CAS Latencies Supported, Most Significant Byte	3
16	Minimum CAS Latency Time (tAmin)	3
1. Number of SPD bytes written will typically be programmed as 128 or 176 bytes. 2. Size of SPD device will typically be programmed as 256 bytes. 3. From DDR3 SDRAM datasheet. 4. These are optional, in accordance with the JEDEC spec.		



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Byte Number	Function Described	Notes
17	Minimum Write Recovery Time (tWRmin)	3
18	Minimum RAS# to CAS# Delay Time (tRCDmin)	3
19	Minimum Row Active to Row Active Delay Time (tRRDmin)	3
20	Minimum Row Precharge Delay Time (tRPmin)	3
21	Upper Nibbles for tRAS and tRC	3
22	Minimum Active to Precharge Delay Time (tRASmin), Least Significant Byte	3
23	Minimum Active to Active/Refresh Delay Time (tRCmin), Least Significant Byte	3
24	Minimum Refresh Recovery Delay Time (tRFCmin), Least Significant Byte	3
25	Minimum Refresh Recovery Delay Time (tRFCmin), Most Significant Byte	3
26	Minimum Internal Write to Read Command Delay Time (tWTRmin)	3
27	Minimum Internal Read to Precharge Command Delay Time (tRTPmin)	3
28	Upper Nibble for tFAW	3
29	Minimum Four Activate Window Delay Time (tFAWmin)	3
30	SDRAM Optional Features	3
31	SDRAM Thermal and Refresh Options	3
32	Module Thermal Sensor	
33	SDRAM Device Type	
34	Fine Offset for SDRAM Minimum Cycle Time (tCKmin)	
35	Fine Offset for Minimum CAS Latency Time (tAmin)	
36	Fine Offset for Minimum RAS# to CAS# Delay Time (tRCDmin)	
37	Fine Offset for Minimum Row Precharge Delay Time (tRPmin)	
38	Fine Offset for Minimum Active to Active/Refresh Delay Time (tRCmin)	
39 ~ 59	Reserved, General Section	
60 ~ 116	Module Type Specific Section, Indexed by Key Byte 3	
117 ~ 118	Module ID: Module Manufacturer's JEDEC ID Code	
119	Module ID: Module Manufacturing Location	
120 ~ 121	Module ID: Module Manufacturing Date	
122 ~ 125	Module ID: Module Serial Number	
126 ~ 127	Cyclical Redundancy Code	
128 ~ 145	Module Part Number	4
146 ~ 147	Module Revision Code	4
148 ~ 149	DRAM Manufacturer's JEDEC ID Code	4
150 ~ 175	Manufacturer's Specific Data	4
176 ~ 255	Open for customer use	
1. Number of SPD bytes written will typically be programmed as 128 or 176 bytes. 2. Size of SPD device will typically be programmed as 256 bytes. 3. From DDR3 SDRAM datasheet. 4. These are optional, in accordance with the JEDEC spec.		